

# “Understanding Nanoelectronics”

AICTE Sponsored

STAFF DEVELOPMENT PROGRAMME

June, 13-25, 2011

Department of Electronic & Communication Engineering

## **Preamble**

Nanoelectronics is nanotechnology applied in the context of electronic circuits and systems.

There are several perspectives to the concept of nanoelectronics.

- One is the fact that the nanoscale dimensions of nanoelectronic components allow for systems of giga-scale complexity measured in terms of component on a chip or in a package. This scaling feature and the road to giga-scale systems can be described as the ‘More Moore’ domain of development;
- Another is that nanotechnology is very diverse and allows the integration of purely electronic devices with mechanical devices, bio-devices, chemical devices, etc. Also, digital systems can be combined with analog/RF circuits. This technology fusion can be described as the ‘More than Moore’ domain of development; and
- A third is that traditional scaling limits in standard CMOS technology are reached during the next decade, calling for fundamentally new nanoscale electronic devices. This development of nanoelectronic components can be denoted the ‘Beyond CMOS’ domain of development.

## **Objectives**

This AICTE supported programme is designed to provide the better understanding of the subject and to provide recent knowledge in nanoelectronics which in turn transferred to students and thus help them to increase employment potential in area of Nano-Electronics Engineering.

**Need:** - In the broadest sense, nanodevices are the critical enablers that will allow mankind to exploit the ultimate technological capabilities of electronic, magnetic, mechanical, and biological systems. While the best examples of nanodevices at present are clearly associated with the information technology industry, the potential for such devices is much broader. Nanodevices will ultimately have an enormous impact on our ability to enhance energy conversion, control pollution, produce food, and improve human health and longevity.

## **Topics to be covered**

- Introduction to Nanoelectronics. Nanotechnology potential.
- Band structure and density of states at Nanoscale.
- Electrical transport in Nanostructure.
- Conduction mechanism in bulk, thin film and low dimensional system.
- Introductory quantum mechanics for Nanoscience.
- Tunnel junction and application of tunneling.
- Quantum wells, wires and dots.
- Single electron transistor: Coulomb Blockade, single electron transistor, other SET and FET structures.
- Ballistic and spin transport: Classical and semi-classical transport, ballistic transport, carbon nanotubes and nanowires, transport of spin and spintronics.
- The era of new Nanostructures of carbon: Buckminsterfullerene, Nanodiamond, BN Nanotubes, Molecular Machine, Nanobiometrics.
- Fabrication technology: Top-down vs bottom-up technology.
- Lithographic process: Lithography, Nanolithography, split gate technology, self assembly, limitation of lithographic process.
- Non-lithographic techniques: Plasma arc discharge, sputtering, evaporation, chemical vapour deposition, pulsed laser deposition, molecular beam epitaxy, sol-gel technique, electrodeposition and other process.

## **Resource Persons**

Prof. (Dr.) Laxmi Narsimhan (East Carolina University, USA)  
Prof. (Dr.) R.K. Pandey (Director, UIT-BU, Bhopal)  
Prof. (Dr.) V.D. Vankar (Professor, IIT- Delhi)  
Prof. (Dr.) E.G. Rajan (Head, Pentagram Research Center, Hyderabad )  
Prof. (Dr.) G.D. Sharma (Professor, Jodhpur University)  
Dr. Anil Kumar (Scientist, CEERI, Pillani)

Dr. Rajnish Kurchania (Associate Professor, MANIT, Bhopal)  
Dr. V Ganeshan (IUC-DI, Indore)  
Prof. (Dr.) R.K. Choudhary (Director, APIIT, Panipat )  
and many more.....

### **Eligibility**

Participants should be faculty members having less than 5 year of experience from Engineering colleges approved by AICTE.

### **Registration Details**

There is no registration fee for the eligible candidates. However, they have to fill-up the registration form and send it to Coordinator on or before 31<sup>st</sup> May 2011, in the given prescribed format. Traveling allowances shall be provided to the eligible participants on producing travel tickets. Free Boarding and Lodging arrangements will be made by the Institute. Certificate, TA and DA will be provided after attending the course for entire duration.

**Note:** To ease the registration process, candidate can confirm there likely participation through mail or telephone. Filling of registration form will be done at the time of reporting.

### **Organizing Committee**

**Patron:** Er. Sanjeev Agrawal ,Chairman SGI

### **Advisors**

Dr. Prashant Jain, Executive Director, SGI  
Dr. Shrihari Agrawal, Group Coordinator, SGI  
Dr. S. C. Bhageria, Director, SIRT  
Dr. V. P. Saxena, Director, SIRT-S  
Dr. Rajiv Shrivastava, Director, SIRT-E  
Dr. M. Kumar, Dean Academic, SIRT  
Prof. P.S. Rajput, Group OSD, SGI  
Prof Ashish Dutta, Group Project Coordinator, SGI

### **Coordinator**

Dr. Akhilesh R. Upadhyay, Vice Principal & HOD, E.C.

### **Contact Detail**

Dr. Akhilesh Upadhyay  
Vice Principal & HOD (E.C.)

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For more details visit us at [www.sirtbhopal.ac.in](http://www.sirtbhopal.ac.in)

### **Important Dates**

Last Date for Registration: 31<sup>st</sup> May, 2011 (Telephonic, Electronically, or Hardcopy)

Workshop: 13<sup>th</sup> June to 25<sup>th</sup> June, 2011

### **Important Contacts**

#### **Registration Committee**

Name :- Miss. Namrata Prasad

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Email:- namrata.prasad7@gmail.com

#### **TA/DA & Certificates**

Name: - Mr, Alok Dubey

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#### **Boarding & Lodging**

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#### **Session Management**

Name :- Mrs. Navneet Kaur

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#### **Local Transport**

Name :- Mr. Ankur Shrivastava

Mobile:-09893512083

E-mail:-ankur\_0407@yahoo.co.in

### **Program Schedule**

Prelaunch Technical Session

Lunch Break

Post lunch Technical Session

9 am to 12 noon

12 noon to 12:30 pm

12:30 pm to 3:30 pm